AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claims 1-8 (canceled).

9. (Currently Amended) A method for serially transmitting data between a first station and a second station, comprising:

transmitting in parallel at least two signals unidirectionally on at least two signal paths, wherein the first station has a first shift register and the second station has a second shift register, each of the first and the second shift registers having at least two register cells corresponding to the at least two signal paths, the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register;

transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by automatically clocking the register cells of the first shift register and the second shift register from a time base directly connected to the register cells, wherein the first shift register and the second shift register are connected by a serial interface, whereby transmission of the at least two signals occurs in real time, wherein each transmitting is performed without loading a CPU;

wherein the automatic clocking is performed at a clock-pulse rate that is at least twice as high as a signal rate that results from a resolution of a signal having the higher resolution between the at least two signals; and

wherein the at least two signals are pulse-width modulated signals.

10. (Canceled).

11. (Canceled).

12. (Canceled).

13. (Canceled).

14. (Currently Amended) ~~The method as recited in Claim 9,~~ A method for serially transmitting data between a first station and a second station, comprising:

transmitting in parallel at least two signals unidirectionally on at least two signal paths, wherein the first station has a first shift register and the second station has a second shift register, each of the first and the second shift registers having at least two register cells corresponding to the at least two signal paths, the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register;

transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by automatically clocking the register cells of the first shift register and the second shift register from a time base directly connected to the register cells, wherein the first shift register and the second shift register are connected by a serial interface, whereby transmission of the at least two signals occurs in real time, wherein each transmitting is performed without loading a CPU;

wherein the automatic clocking occurs at a clock-pulse rate, and a cycle time resulting from the clock-pulse rate is one of less than and equal to a slope time of the at least two signals transmitted; and

wherein the at least two signals are pulse-width modulated signals.

15. (Currently Amended) A system for serially transmitting data between a first and a second station, comprising:

a first station having a first shift register with at least two register cells;

a second station having a second shift register with at least two register cells;

a serial interface connecting the first shift register and the second shift register; and

a time base directly connected to the register cells of the first and second shift registers;

wherein at least two signals are unidirectionally routed in parallel on at least two signal paths into the at least two register cells of the first shift register, and wherein data corresponding to the at least two signals are serially transmitted from the first shift register to the second shift register by automatically clocking the register cells of the first shift register and the second shift register from the time base, whereby transmission of the at least two signals occurs in real time and are performed without loading a CPU;

wherein the time base is a timer module that automatically generates a time signal at fixed intervals;

wherein the automatic clocking occurs at a clock-pulse rate, and a cycle time resulting from the clock-pulse rate is one of less than and equal to a slope time of the at least two signals transmitted; and

wherein the at least two signals are pulse-width modulated signals.

16. (Canceled).